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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/399,510	09/20/1999	KIMBLE DONG	384938007US	2349

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EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2612	14

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Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/399,510	Applicant(s) DONG ET AL.	
	Examiner Justin P Misleh	Art Unit 2612	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 June 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ they raise the issue of new matter (see Note below);
   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____.
3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: *6*.

   Claim(s) rejected: *1 - 3, 6, 7, and 10*.

   Claim(s) withdrawn from consideration: _____.
8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.
9. ☒ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). *13*.
10. ☐ Other: _____

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SUPERVISORY PATENT EXAMINER
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Continuation of 5. does NOT place the application in condition for allowance because:

In a first issue, the Applicant states, "The Examiner's arguments that 'divided voltage value' is a second voltage level is erroneous. The divided voltage value is simply the analog version of the digital signal input in the D/A converter 250. They are not two different voltage levels as required by the claims, but rather digital and analog versions of the same voltage level."

The Examiner disagrees with the Applicant's position.

First, it is important to note that in the Final Office Action (Paper No. 11, 19 May 2004), the Examiner stated, in regards to the rejection of Claim 1 (page 4, Paragraph 7), that the first set voltage level is voltage level B from the microcomputer. Kim states the following in regards to voltage level B from the microcomputer (see column 3, lines 18 – 22 and 57 – 60): "a digital comparator 230 for comparing a black level of the digital image signal outputted from the A/D converter 210 with a black level calibration value received from a microcomputer and outputting a compared resultant value accordingly" and "the digital comparator 230 compares the black level value A of the digital image signal received from the A/D converter 210 with a previously set black level calibration value B received from the microcomputer." Therefore, it is clear that voltage level B is set from the microcomputer and is identified as the first set voltage level. (emphasis added).

Second, it is important to note that in the Final Office Action, the Examiner stated, in regards to the rejection of Claim 1 (page 5, also Paragraph 7 continued), that the second set voltage level is the divided voltage value selected from a plurality of divided voltage by the D/A Converter. Kim states the following in regards to the selected divided voltage value (see column 4, lines 14 – 16 and 56 – 62): "the D/A converter 250 includes a decoder 251 for decoding the n-bit digital control signal to 2.sup.n bits" and "the respective switches S1.about.S2.sup.n of the divided voltage selector 253 become turned on/off in accordance with the digital control signal received from the decoder 251 so that one of the voltages divided in the voltage divider 252 is selected and outputted accordingly, and the output signal of the divided voltage selector 253 is amplified to an appropriate level through the output buffer 254." Therefore, it is clear that the divided voltage value is derived from the n-bit digital control signal. (emphasis added)

Third, it is important to note the relationship between the first set voltage level (voltage level B), the second set voltage level (divided voltage value), and the n-bit control signal. This is what Kim states (see column 3, line 57 through column 4, line 9): "the digital comparator 230 compares the black level value A of the digital image signal received from the A/D converter 210 with a previously set black level calibration value B received from the microcomputer. If A>B, a 'high' signal is outputted to the up/down counter 240, if A=B, an 'IN' signal is outputted to the up/down counter 240, and if A<B, a 'low' signal is outputted to the up/down counter 240. The up/down counter 240 raises or lowers a present count value depending upon an output signal of the digital comparator 230. For example, when the output signal of the digital comparator 230 is at a high level, the present count value is lowered by "one", if at the low level, the present count value is raised by "one", and if at "IN", the count value remains unchanged, that is, the present count value is fixed. The thusly determined n-bit control signal is applied to the D/A converter 250, and the D/A converter 250 increases or decreases the lower phase reference voltage V.sub.B generated by the reference voltage generator 220 in accordance with the n-bit control signal." (emphasis added)

Therefore, the first set voltage level (voltage level B) and the second set voltage level (divided voltage value) are NOT digital and analog versions of the same voltage level as argued by the Applicant.

In a second issue, the Applicant argues, "While the Kim patent discloses an automatic gain control block 200, there is no indication that the automatic gain control block 200 can be adjusted in any manner, let alone be adjusted base upon the use of a second counter as is required in Claims 1 and 7." Furthermore, the Applicant argues, "The Kim patent does not address the modification of the automatic gain control at all."

Again, the Examiner disagrees with the Applicant's position.

Kim's invention is a black level calibration apparatus that celebrates the black level of an input image signal using a feedback loop. Kim's black level calibration apparatus remains in the feedback loop until the black level of the digital image signal (A) is identical to the black level digital reference level (B), as stated in column 5 (lines 11 – 16). The Examiner will now step through the feedback loop disclosed by Kim in figure 1:

In a first iteration of the feedback loop, a first processed pixel signals are output from CDS/AGC 200 and input into the A/D Converter 210 to create a first digital image signal. The first digital image signal is output from the A/D Converter 210 and input into Digital Comparator 230, which compares the first processed pixel signals/digital image signals to a first set voltage level (voltage level B). As stated above, the first set voltage level is voltage level B from the microcomputer. Up/Down Counter 240 maintains a first count according to the guidelines set forth in column 3, line 60, through column 4, line 4. The first count is representative of the number of pixels of the first processed pixel signals/digital image signal that are above and/or below the first set voltage level. The first count, which is an n-bit digital control signal, is input into the D/A Converter 250. The D/A Converter 250 accepts two inputs, one of which is the n-bit digital control signal (first count) and the other of which is a lower phase reference voltage VB generated in reference voltage generator 220. The D/A Converter 250 divides the lower phase reference voltage VB into a lesser voltage according to the n-bit digital control signal (first count). As stated above, the second set voltage level is the divided voltage level (VB by n-bit) divided by D/A Converter 250.

The divided voltage level (second set voltage level) is input into the Black Level Clamp Circuit 260. The Black Level Clamp Circuit 260 accepts two inputs, one of which is the divided voltage level (second set voltage level) and the other of which is the first processed pixel signals/digital image signal so as clamp the black level of the image signal. The first clamped image signal is fed back to the CDS/AGC 200 wherein the first clamped image signal modifies the CDS/AGC processing at the beginning of the second iteration.

In a second iteration of the feedback loop, a second processed pixel signals that have been processed according to the clamped image signals input as feedback are output from CDS/AGC 200 and input into the A/D Converter 210 to create a second digital image signal. The second digital image signal is output from the A/D Converter 210 and input into Digital Comparator 230, which compares the second processed pixel signals/digital image signals to again a first set voltage level (voltage level B). As stated above, the first set voltage level is voltage level B from the microcomputer. Up/Down Counter 240 maintains a second count according to the guidelines set forth in column 3, line 60, through column 4, line 4. The second count is representative of the number of pixels of the second processed pixel signals/digital image signal that are above and/or below the first set voltage level. The second count, which is an n-bit digital control signal, is input into the D/A Converter 250. The D/A Converter 250 accepts two inputs, one of which is the n-bit digital control signal (first count) and the other of which is a lower phase reference voltage VB generated in reference voltage generator 220. The D/A Converter 250 divides the lower phase reference voltage VB into a lesser voltage according to the n-bit digital control signal (second count). As stated above, the third set voltage level is the divided voltage level (VB by n-bit) divided by D/A Converter 250. The divided voltage level (third set voltage level) is input into the Black Level Clamp Circuit 260. The Black Level Clamp Circuit 260 accepts two inputs, one of which is the divided voltage level (third set voltage level) and the other of which is the second processed pixel signals/digital image signal so as clamp the black level of the image signal. The second clamped image signal is fed back to the CDS/AGC 200 wherein the second clamped image signal modifies the CDS/AGC processing at the beginning of the third iteration.

Therefore, according to the Examiner's interpretation of Kim, Kim provides a first set voltage leave and second set voltage level, which are different from each other. Furthermore, Kim provides a first count in a first iteration and a second count in a second iteration wherein by means of a d/a converter and a black level clamping circuit, the second count is used to determine a second digital control signal for adjusting the amplification of the process pixel signals.